# Silicon Validation of Evolution-Designed Circuits

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## Abstract

*No silicon fabrication and characterization of circuits with topologies designed by evolution has been done before, leaving open questions about the feasibility of the evolutionary design approach, as well as on how high-performance, robust, or portable such designs could really be when implemented in hardware. This paper is the first to report on a silicon implementation of circuits evolved in simulation. Several circuits were evolved and fabricated in 0.5-micron CMOS process; this paper focuses on results of logical gates evolved at transistor level. It discusses the steps taken in order to increase the chances of robust and portable designs, summarizes the results of characterization tests based on chip measurements, and comments on the performance comparing to simulations.*

## 1. Introduction

Conventional design techniques explore only a small fraction of the design space, relying on validated circuit topologies, assembling them as building blocks for achieving overall functionality, and optimizing their parameters for process portability and increased performance.

Beyond these techniques, one notices the appearance of unconventional design techniques, which challenge the very foundation of modern design based on *design-reuse*, revisiting the traditional building blocks, often achieving a full *on-demand design*, unique, perhaps with never-used before topologies. The downside to these techniques is the lack of silicon validation that gives confidence to designers about how their circuits would behave when fabricated in real hardware.

Evolutionary circuit design [1], [2], [3], enters this category, allowing the exploration of a larger fraction of the design space compared to conventional tools [2]. The power of evolutionary algorithms to do complete topological synthesis has been proven before [3], [5], [6]. One of the challenges relates mainly to the scalability of the approach, which in our experience appears to not be able to address designs requiring over ~100 components. Designs that are more complex could still be addressed if one increases the complexity of the components. Other solutions to scalability are also under investigation [7].

Another potential limitation of evolutionary circuit design is true for all unconventional design techniques: an issue of confidence that the solution will actually work in silicon as predicted by simulations. Naturally, the lack of characterization resulting from previous tested "sub-circuits" impedes using such data in simulation models. Perhaps one of the outcomes of these explorations of non-conventional techniques will be an extension of the class of circuits currently in use (human-designed), with new, machine designed circuits, which would however be used in the future as common building blocks for larger circuits.

The solution obtained by evolutionary design may work for the narrow domain where commonly tested (since full domain testing is at least impractical, often impossible). It may work for a targeted process and fail on another. This portability aspect was first noted since earliest evolutionary experiments of Thompson [4], in which case a solution evolved in one FPGA (with the hardware in the loop) failed to work in the same way when tried on another similar FPGA, or even on different part of the same FPGA. This is strongly related to differences in the set of characteristics that evolution exploited in one FPGA chip and could not exploit in the other FPGA. Particularly, for evolutions with the chip in

the loop, evolution can explore subtle properties of the silicon, and parasitic effects, which vary even between 'identical' chips.

The same has been noted when evolving in simulations and then attempting to map the result to programmable hardware. This worked in some situations but it did not work on others. The reverse was also observed: circuits evolved on a programmable device did not always work the same way in a simulation of the topology (see [8] for more details). The solution proposed in [8] was mixtrinsic evolution, evaluating candidate solutions both in software and in hardware, in same generation or alternating over generations. This solution works only for reconfigurable devices. The mixtrinsic technique was extended in [9] to include mixtures of software-only models, such as models of different resolution, models of various processes or different analysis tests, etc. This technique was applied in the work described here as a mean to increase the reliability and robustness of evolved designs.

No silicon implementation of a circuit designed by evolution has been reported to date (we refer here to an ASIC solution rather than evolved solution mapped on a programmable device as in our FPTA experiments [8], or a configuration/routing solution using conventional FPGA cells [10]). Perhaps the lack of performance of unconventional evolved designs, which are still in the "proof-of-concept" mode, or perhaps the lack of trust in their performance after fabrication (due to limitations of simulators or simulation models, simplifications to render evolution practical, such as testing only on certain operational points) deterred researchers from risking fabrication costs.

The focus of this paper is on presenting methods that were found useful in evolutionary *design-for-fabrication* and showing silicon results. It presents the first case in which circuits evolved in simulations were fabricated in silicon as a test ASIC and characterized. The test chip had several evolved circuits; only measurements of evolved logical circuits and an adder made with these gates is shown here. The paper is organized as follows: section 2 summarizes methods used to increase portability/robustness of evolved circuits. Section 3 presents responses measured in silicon, and compares with simulation. Section 4 presents conclusions.

## 2. Methods used in evolutionary design-for-fabrication

Comprehensive testing is needed to ensure that evolved solutions would cover the intended operational space; no assumptions on their performance outside the points tested during evolution could be reliably made. The methods described below proven useful in obtaining circuits that satisfied the requirements and functioned as predicted in silicon.

1) Candidate logic circuits were tested in transient analysis for all possible transitions of combinations of input levels, as opposed to all possible levels in only one order. (For example a circuit may respond well as an AND gate to input combinations of levels 0-0, 0-1, 1-0, 1-1. However, it may turn out to have a too long discharge time when tested with the combination of inputs 1-1 following 0-0 - and not 1-0 as above, which is not tested in the simple scheme). The price to pay is increased transient analysis duration. Thus, even for four different input combinations for the operating point analysis in a 2-input gate, transient analysis used seven input configuration cases (for the gates studied here) to include all the combination sequences (fig. 5 shows an example).

2) Circuits were tested on various loads including loading of copies of itself (identical circuits) to guarantee that it will be able to drive similar gates. This is a way to ensure both that the circuit would drive others like it, as well that the circuit can be driven by others (both input and output impedance aspects are addressed this way). Driving a fixed load may not be optimal since we don't know anything in advance about input or output impedance of the circuit to be designed, unless it is a design requirement. This avoids problems we noticed in preliminary experiments of not being able to drive similar circuits.

3) Domain knowledge was used to speed up evolution of circuits with good loading capability. We constrained evolution into using only transistor gates to connect circuit inputs (preventing input connections to transistor source or drain), thereby forcing high input impedance of the evolving circuit gate. This greatly shortened the time for evolving cascaded circuits.

4) Testing at several frequencies was used as opposed to testing only at one. The implicit assumption of human designers that a circuit should function at various frequencies may be missing from explicitly formulated requirements and thus from the fitness function of an evolutionary design. An example is the implicit assumption that a logic gate should have the same behavior over a "frequency range" i.e. function with slow/DC signals as well as faster input changing signals. Simplistic testing would use an input stimulus with a SPICE transient analysis with changes in the microsecond range, and correct behavior for this timescale would be quickly achieved by evolution. However, this circuit may have a totally different behavior at a different timescale. Circuits required to be fast, may not work on DC levels (we evolved several of this circuits which work if inputs switch faster than a charge is eliminated). Similarly, circuits evaluated at a slow timescale evolution will result in slow gates: so evaluations at both domains are needed. This is an example of mixtrinsic evolution, in which same circuit is evaluated not on two or more models, but with two or more analysis types.

The above approach may lead to extensive simulation time for evaluations. One way to address this is to extend the transient analysis duration to avoid transient solutions (with wrong behavior at large timescales) while keeping the transient analysis step small enough to assess the gate speed.

5) Accelerated evolution via mixtrinsic evolution, biasing the population to more individuals evaluated with a simplified (faster to simulate) SPICE model. For example, we used a level-3 transistor model for the HP 0.5-micron process to simulate faster than the BSIM model given by the manufacturer. At one extreme, the population consists only of circuits evaluated with the simplified model, however in such cases we simulated again all solution circuits using the complete BSIM models and their design corners (using both slow and fast versions of the HP model). In our experiments, the simplified transistor model delivered sufficiently accurate results in the case of logic gates when compared to the silicon measurements. This will certainly prove wrong for designs pushing the limits of performance (e.g. very high frequencies).

6) Use mixtrinsic evolution to speed-up evolution for robustness to changes in temperature and power supply (Vdd). Again, we have the choice of skewing the distribution of population in mixtrinsic search, from populations in which all individuals go through full testing (at the cost of an increase in the evolution time), to populations in which few or none go to all testing and most or all go to simplified testing and only the final evolved circuits are tested to all design corners. In our experiments most (but not all) of the solution circuits achieved through partial testing worked for ± 10% variations of Vdd and a wide range of temperatures (–20$^{o}$C to 200$^{o}$C). In this case it was convenient to evolve the circuits for nominal conditions and test the final solution for the design corners, but again this may not be necessarily the fastest way.

## 3. Silicon validation results

Several circuits were evolved at transistor level with the technique detailed in [5] and then were fabricated on a prototype ASIC on a HP 0.5 micron process. The chromosome encodes the circuit topology (MOS transistor connections) and the transistors' sizes (width and length). In most experiments, the number of components was imposed or restricted to maximum 8. Most experiments used populations of 40 individuals and a number of 400 generations.

Figure 1 depicts the response of an evolved NAND gate and Figure 2 shows the response of an evolved NOR gate.

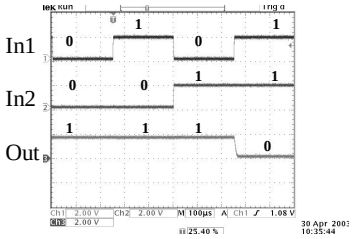


**Figure 1: Evolved NAND gate response as measured in silicon.**

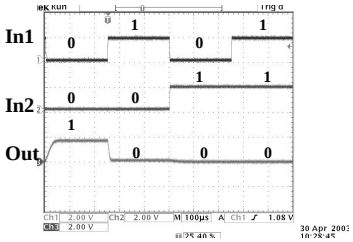


**Figure 2: Evolved NOR gate response as measured in silicon.**

These responses prove the correct functionally in silicon of the evolved designs, and agree very well with the simulations. With one exception, this was true for all circuits. In only one case was there a discrepancy, in which we discovered that only the simplified model was used and we did not check the foundry model; a mistake that once more proves the need for thorough evaluation of evolved circuits.

To illustrate their operability in cascaded designs, an error detection adder was also fabricated on the same chip. This demonstrated that the evolved NAND gate can be cascaded to build more complex digital circuits. Figure 3 depicts the adder schematic and Figure 4 shows its measured response.

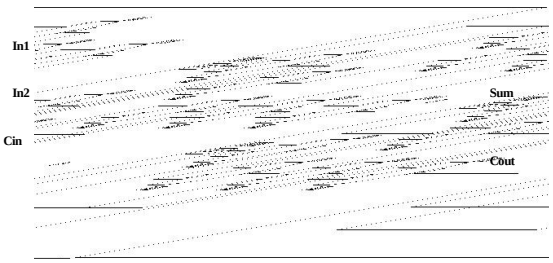


**Figure 3: Schematic of Adder circuit based on evolved NAND gate (Figure 1). Inputs are In1, In2 and Carry-in (Cin) . Outputs are Sum and Carry-Out (Cout).**

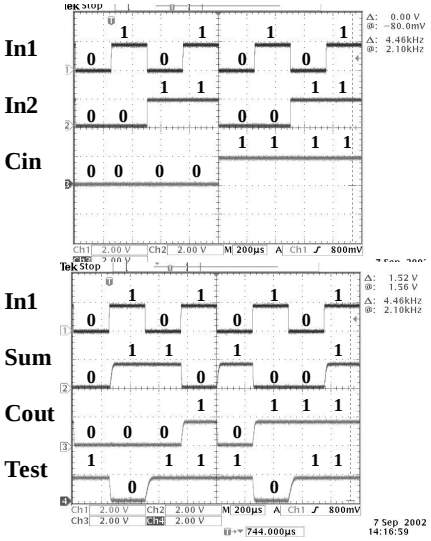


**Figure 4: Adder response as measured in silicon. (Test output is an internal test point).**

## 4. Conclusions

This paper presented the first case of silicon validation of evolution-designed circuits. It presented several design-for-fabrication recommendations for evolutionary design. It illustrated results of silicon measurements for logic gates evolved from transistors. It illustrated the usability of these evolution-designed blocks into more complex designs, with an adder made of evolved gates. It illustrated the point that no predictability of behavior outside the tested range in simulations (during evolution or for the result of evolution) is realistic.

## Acknowledgements

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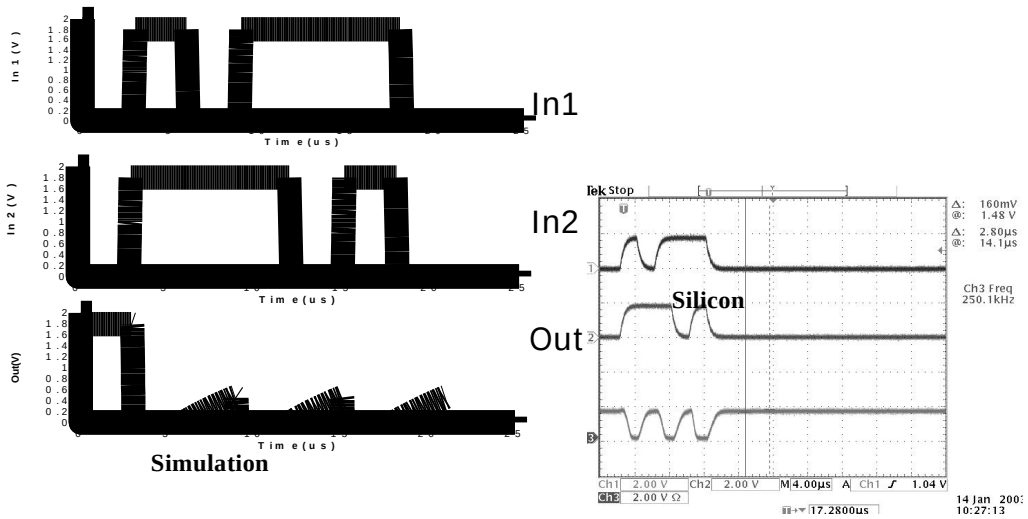


**Figure 5: Evolved NAND gate tested for 2μs switching period: simulation in the left and silicon measurements in the right.**

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